AF/2188

# TRANSMITTAL FORM

*(to be used for all correspondence after initial filing)*

| | |
|---|---|
| Application No. | 09/822,643 |
| Filing Date | March 30, 2001 |
| First Named Inventor | Blaise Fanning |
| Art Unit | 2188 |
| Examiner Name | Gary J. Portka |
| Total Number of Pages in This Submission | 54 |
| Attorney Docket Number | 42390P10572 |

**ENCLOSURES** ***(check all that apply)***

- [x] Fee Transmittal Form
  - [x] Fee Attached
- [ ] Amendment / Response
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
  - [ ] PTO/SB/08
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
  - [ ] Basic Filing Fee
  - [ ] Declaration/POA
- [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s)
- [ ] After Allowance Communication to Group
- [ ] Appeal Communication to Board of Appeals and Interferences
- [x] Appeal Communication to Group **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
- [ ] Status Letter
- [x] Other Enclosure(s) *(please identify below):*

- Two copies of Appeal Brief



Remarks

**SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT**

| | |
|---|---|
| Firm *or* Individual name | Thinh V. Nguyen, Reg. No. 42,034<br>BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP |
| Signature | |
| Date | July 1, 2004 |

**CERTIFICATE OF MAILING/TRANSMISSION**

I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Appeal, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

| | | | |
|---|---|---|---|
| Typed or printed name | **Tu T. Nguyen** | | |
| Signature | | Date | **July 1, 2004** |

# FEE TRANSMITTAL for FY 2004

*Effective 01/01/2004. Patent fees are subject to annual revision.*

☐ Applicant claims small entity status. See 37 CFR 1.27.

**TOTAL AMOUNT OF PAYMENT** ($) 330.00

| *Complete if Known* | |
|---|---|
| Application Number | 09/822,643 |
| Filing Date | March 30, 2001 |
| First Named Inventor | Blaise Fanning |
| Examiner Name | Gary J. Portka |
| Art Unit | 2188 |
| Attorney Docket No. | 42390P10572 |

## METHOD OF PAYMENT *(check all that apply)*

☒ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☐ Deposit Account

Deposit Account Number: 02-2666

Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP

**The Commissioner is authorized to:** *( check all that apply)*

☐ Charge fee(s) indicated below ☒ Credit any overpayments

☒ Charge any additional fee(s) or underpayment of fees as required under 37 CFR §§ 1.16, 1.17, 1.18 and 1.20.

☐ Charge fee(s) indicated below, **except for the filing fee** to the above-identified deposit account

## FEE CALCULATION

### 1. BASIC FILING FEE

| Large Entity Fee Code | Large Entity Fee ($) | Small Entity Fee Code | Small Entity Fee ($) | Fee Description | Fee Paid |
|---|---|---|---|---|---|
| 1001 | 770 | 2001 | 385 | Utility filing fee | |
| 1002 | 340 | 2002 | 170 | Design filing fee | |
| 1003 | 530 | 2003 | 265 | Plant filing fee | |
| 1004 | 770 | 2004 | 385 | Reissue filing fee | |
| 1005 | 160 | 2005 | 80 | Provisional filing fee | |

SUBTOTAL (1) ($)

### 2. EXTRA CLAIM FEES

| | | | Extra Claims | | Fee from below | Fee Paid |
|---|---|---|---|---|---|---|
| Total Claims | | - 32** = | | X | | = |
| Independent Claims | | - 3 = | | X | | = |
| Multiple Dependent | | | | | | = |

| Large Entity Fee Code | Large Entity Fee ($) | Small Entity Fee Code | Small Entity Fee ($) | Fee Description |
|---|---|---|---|---|
| 1202 | 18 | 2202 | 9 | Claims in excess of 20 |
| 1201 | 86 | 2201 | 43 | Independent claims in excess of 3 |
| 1203 | 290 | 2203 | 145 | Multiple Dependent claim, if not paid |
| 1204 | 86 | 2204 | 43 | **Reissue independent claims over original patent |
| 1205 | 18 | 2205 | 9 | **Reissue claims in excess of 20 and over original patent |

SUBTOTAL (2) ($)

***or number previously paid, if greater, For Reissues, see below*

## FEE CALCULATION (continued)

### 3. ADDITIONAL FEES

| Large Entity Fee Code | Large Entity Fee ($) | Small Entity Fee Code | Small Entity Fee ($) | Fee Description | Fee Paid |
|---|---|---|---|---|---|
| 1051 | 130 | 2051 | 65 | Surcharge - late filing fee or oath | |
| 1052 | 50 | 2052 | 25 | Surcharge - late provisional filing fee or cover sheet. | |
| 2053 | 130 | 2053 | 130 | Non-English specification | |
| 1812 | 2,520 | 1812 | 2,520 | For filing a request for *ex parte* reexamination | |
| 1804 | 920* | 1804 | 920* | Requesting publication of SIR prior to Examiner action | |
| 1805 | 1,840* | 1805 | 1,840* | Requesting publication of SIR after Examiner action | |
| 1251 | 110 | 2251 | 55 | Extension for reply within first month | |
| 1252 | 420 | 2252 | 210 | Extension for reply within second month | |
| 1253 | 950 | 2253 | 475 | Extension for reply within third month | |
| 1254 | 1,480 | 2254 | 740 | Extension for reply within fourth month | |
| 1255 | 2,010 | 2255 | 1,005 | Extension for reply within fifth month | |
| 1404 | 330 | 2401 | 165 | Notice of Appeal | |
| 1402 | 330 | 2402 | 165 | Filing a brief in support of an appeal | 330.00 |
| 1403 | 290 | 2403 | 145 | Request for oral hearing | |
| 1451 | 1,510 | 2451 | 1,510 | Petition to institute a public use proceeding | |
| 1452 | 110 | 2452 | 55 | Petition to revive - unavoidable | |
| 1453 | 1,330 | 2453 | 665 | Petition to revive - unintentional | |
| 1501 | 1,330 | 2501 | 665 | Utility issue fee (or reissue) | |
| 1502 | 480 | 2502 | 240 | Design issue fee | |
| 1503 | 640 | 2503 | 320 | Plant issue fee | |
| 1460 | 130 | 2460 | 130 | Petitions to the Commissioner | |
| 1807 | 50 | 1807 | 50 | Processing fee under 37 CFR 1.17(q) | |
| 1806 | 180 | 1806 | 180 | Submission of Information Disclosure Stmt | |
| 8021 | 40 | 8021 | 40 | Recording each patent assignment per property (times number of properties) | |
| 1809 | 770 | 1809 | 385 | Filing a submission after final rejection (37 CFR § 1.129(a)) | |
| 1810 | 770 | 2810 | 385 | For each additional invention to be examined (37 CFR § 1.129(b)) | |
| 1801 | 770 | 2801 | 385 | Request for Continued Examination (RCE) | |
| 1802 | 900 | 1802 | 900 | Request for expedited examination of a design application | |

Other fee (specify) _____

* Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 330.00



## SUBMITTED BY

Complete (if applicable)

| Name (Print/Type) | Thinh V. Nguyen | Registration No. (Attorney/Agent) | 42,034 | Telephone | (714) 557-3800 |
|---|---|---|---|---|---|
| Signature | | | | Date | 07/01/04 |

Based on PTO/SB/17 (10-03) as modified by Blakely, Sokoloff, Taylor & Zafman (wlr) 02/10/2004.
SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Docket No.: 042390.P10572

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

| | |
|---|---|
| In re Application of:<br>Blaise B. Fanning<br>Application No.: 09/822,643<br>Filed: March 30, 2001<br>For: CONTROLLING CACHE MEMORY IN EXTERNAL CHIPSET USING PROCESSOR | Examiner: Gary J. Portka<br><br>Art Group: 2188 |

APPEAL BRIEF



Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicant submits, in triplicate, the following Appeal Brief pursuant to 37 C.F.R. § 1.192 for consideration by the Board of Patent Appeals and Interferences. Applicant also submits herewith our check number ***31283*** in the amount of $330.00 to cover the cost of filing the opening brief as required by 37 C.F.R. § 1.17(f). Please charge any additional fees or credit any overpayment to our deposit Account No. 02-2666. A duplicate copy of the Fee Transmittal is enclosed for this purpose.

07/08/2004 RMEBRAHT 00000075 09822643
01 FC:1402 330.00 OP

## TABLE OF CONTENTS

## I. REAL PARTY IN INTEREST

The real party in interest is the assignee, Intel Corporation.

## II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to the appellants, the appellants' legal representative, or assignee, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

## III. STATUS OF CLAIMS

Claims 1-32 of the present application are pending and remain rejected. The Applicant hereby appeals the rejection of claims 1-32.

## IV. STATUS OF AMENDMENTS

The Applicant filed an amendment on March 31, 2004, in response to a Final Office Action issued by the Examiner on February 11, 2004. In response to the March 31, 2004 amendment, the Examiner issued an Advisory Action on April 21, 2004. The Applicant filed a Notice of Appeal from the Advisory Action issued by the Examiner on May 11, 2004.

## V. SUMMARY OF INVENTION

The invention is a technique to control cache memory in external chipset using the processor. A computer system 100 includes, among other things, a processor 110, a memory control hub (MCH) 130, a system memory 140, and an input/output control hub (ICH) 150.[1]

The processor 110 includes a processor core 112 and a cache unit 115. The processor core 112 performs necessary processor operations such as fetching instruction and data, decoding instructions, and executing the instructions. The cache unit 115

[1] Specification, page 3, lines 9-14.

provides an internal cache (e.g., level I) or processor cache and a control mechanism for an external cache (e.g., level II).[2]

The MCH 130 provides control and configuration of memory and input/output devices such as the system memory 140 and the ICH 150. The MCH 130 includes a chipset cache 135. The chipset cache 135 is the external cache (e.g., level II) to store cache information. By moving the control functions including the cache tag store out of the MCH 130 and into the processor 110, significant saving in hardware can be achieved. In addition, the processor 110 can perform control functions and maintain cache coherence logic in a more efficient manner.[3]

The cache unit 115 includes a processor cache unit 210, a chipset cache controller 240, and a snoop circuit 270.[4]

The processor cache unit 210 maintains the internal cache (e.g., level I) for the processor 110 and processes a cache access request from the processor core 112. The processor cache unit 210 includes a processor cache controller 220 and a processor cache 230. The processor cache request may be a read or a write request. The processor cache unit 210 also interfaces with the snoop circuit 270 to manage and maintain cache coherency for the system. The processor cache controller 220 controls the processor cache 230.[5]

The chipset cache controller 240 controls the chipset cache 135 located in the chipset MCH 130 in response to the cache access request from the processor core 112. By implementing the control functions of the external cache inside the processor 110, the cache management and coherence control can be performed efficiently. The chipset cache controller 240 includes a chipset cache tag store 250 and a coherence controller 260.[6]

The chipset cache tag store 250 stores the tags associated with the cache lines in the chipset cache 135. The coherence controller 260 maintains cache coherency among the processor cache 230, the chipset cache 135, and the memory 140 according to a coherence protocol. The coherence controller 260 includes a chipset interface circuit 265 to send control signals 280 to the chipset MCH 130 according to the cache state and the type of the

[2] Specification, page 3, lines 22-25; page 4, lines 1-3.
[3] Specification, page 4, lines 18-24.
[4] Specification, page 6, lines 7-9.
[5] Specification, page 6, lines 10-17.
[6] Specification, page 7, lines 3-9.

cache access request (e.g., read access, write access). The control signals 280 specify an operation performed by the chipset 130.[7]

The control signals 280 include at least a set identifier, a cache valid indicator, and a flush indicator.[8] The control signals may be sent to the chipset MCH 130 via some pins on the processor 110 along with the standard address cycle during the request and/or snoop phase. The signals may be sent out on the processor pins that are double-pumped. They may also be whispered to the chipset 130 by quad-pumping the address communication. Double and quad pumpings refer to the clocking scheme that strobes the data twice and four times, respectively, faster than the bus clock signal.[9]

The snoop circuit 270 snoops the bus 120 to monitor any address information sent by other bus masters in the system as part of the system cache coherency management. The snoop circuit 270 checks if an address snooped on the bus 120 matches with one of entries in the chipset cache tag store 250. The snoop circuit 270 may also forward the snooped address to the processor cache unit 210 for cache coherence maintenance. The set identifier in the control signals may also specify the cache set corresponding to the one of the entries that matches the address snooped on the bus.[10]

## VI. ISSUES

The issues are:

(1) whether claims 1-2, 14-15, and 27-28 are obvious under 35 U.S.C. §103(a) over U.S. Patent No. 6,237,064 issued to Kumar et al. ("Kumar") in view of U.S. Patent No. 6,047,348 issued to Lentz et al. ("Lentz"), and

(2) whether claims 3-13, 16-26, 29-32 are obvious under 35 U.S.C. §103(a) over Kumar in view of U.S. Patent No. 6,629,218 issued to Cho ("Cho"), further in view of Lentz, and further in view of U.S. Patent No. 6,438,657 issued to Gilda ("Gilda").

[7] Specification, page 7, lines 10-20.
[8] Specification, page 7, lines 20-21.
[9] Specification, page 8, lines 5-15.
[10] Specification, page 8, lines 16-22.

## VII. GROUPING OF CLAIMS

Applicant submits that the claims of the present invention form into two groups. Group 1 includes claim 1-2, 14-15, and 27-28 and Group 2 includes claims 3-13, 16-26, 29-32.

## VIII. ARGUMENTS

### A. Claims 1-2, 14-15, and 27-28 Are Not Obvious Under Kumar In View Of Lentz

In the final Office Action dated February 11, 2004, the Examiner rejected claims 1-2, 14-15, and 27-28 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,237,064 issued to Kumar et al. ("Kumar") in view of U.S. Patent No. 6,047,348 issued to Lentz et al. ("Lentz"). Applicant respectfully traverses the rejection and contends that the Examiner has not met the burden of establishing a prima facie case of obviousness. To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *MPEP §2143, p. 2100-129 (8th Ed., rev. 2, May 2004).* Applicant respectfully contends that there is no suggestion or motivation to combine their teachings, and thus no *prima facie* case of obviousness has been established.

Kumar discloses a cache memory with reduced latency by paralleling various memory accesses initiated by the execution unit (Kumar, col. 3, lines 42-44). A first cache, a second cache, and a tag array of a third cache are resident in the processor core (Kumar, col. 3, lines 9-13). However, Kumar does not disclose or suggest the cache to be internal to a memory controller.

Cho discloses an out of order associative queue in two clock domains. A system includes two processors, an L2 cache, a memory controller, a pair of input/output (I/O) bridges, and I/O interfaces (Cho, col. 3, lines 14-16). The processors, the L2 cache, the memory controller, the I/O interfaces, the I/O bridges, and the bus may be integrated onto a single integrated circuit as a system on a chip configuration (Cho, col. 5, lines 38-42). Any

level of integration may be used (Cho, col. 5, line 47). However, Cho doe not disclose or suggest a cache to be internal to a memory controller which is external to the processor.

Lentz discloses a system and method for supporting a multiple width memory subsystem. A subsystem writes to a main memory by either a 32 or 64 bit data transfer. It transfers data in a "double pumped" fashion (Lentz, col. 4, lines 61-64). Lentz merely discloses double pumping data bus, not control signals. Lentz even states that double pumping may cause bus conflict when the buses turn around and switch from one master to a new master (Lentz, col. 5, lines 1-4). This indicates that Lentz does not suggest to use double pumping for control signals.

Kumar, Cho, and Lentz, taken alone or in any combination, does not disclose, suggest, or render obvious controlling a cache memory in a memory controller via double-pumped or quad-pumped control signals. There is no motivation to combine Kumar, Cho, and Lentz, because none of them addresses the problem of controlling a cache memory in a memory controller using a controller internal to a processor. There is no teaching or suggestion that the control signals being double pumped or quad-pumped is present. Kumar, read as a whole, does not suggest the desirability of putting the chipset cache in a memory controller. Lentz merely discloses double pumping data signals, not control signals.

Furthermore, if the proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). MPEP 2143.01.

Here, Kumar does not disclose or suggest the external cache being internal to a memory controller which is external to the processor. Moving the cache into the memory controller would render Kumar's circuit unsatisfactory for its intended purpose. The intended purpose of Kumar's technique is to reduce cache latency by paralleling various memory accesses by the execution unit (Kumar, col. 3, lines 42-44). Kumar specifically provides two separate buses: a backside bus (BSB) and a frontside bus (FSB) associated with a BSB queue and a FSB queue, respectively (Kumar, col. 5-8). Kumar further teaches that the BSB queue tracks the memory requests submitted to the offchip L2 data array of the L2 cache, while the FSB queue tracks the memory requests submitted to the main memory (Kumar, col. 4, lines 9-13). Therefore, Kumar does not suggest to incorporate the

L2 cache inside the memory controller because that would defeat the purpose of parallel operations.

In the Advisory Action dated April 21, 2004, the Examiner stated that "[t]he parallel access, as argued, in Kumar would still be provided by the parallel access of L0 and L1 (Kumar, col. 3, lines 41-51)". This argument is fundamentally flawed. First the rejected claims recite a chipset cache controller internal to a processor to control a chipset cache external to the processor (e.g., an L2 cache). See, for example, Specification page 4, lines 19-20. In the final Office Action dated February 21, 2004, the Examiner focused the rejection on the L2 cache and stated that "Kumar does not disclose that the L2 cache is part of a memory controller." (Final Office Action, page 3, paragraph 6). The issue is, therefore, whether placing L2 in the memory controller still serves the purpose of parallel access to the L2 cache and the memory, not whether there is a parallel access to L0 and L1. Second, L0 and L1 are both internal caches, not external cache, and not inside a memory controller. The rejected claims do not recite internal cache. Therefore, moving the L2 cache into the memory controller would render Kumar's circuit unsatisfactory for its intended purpose of having parallel access via the backside bus and the frontside bus.

Cho merely discloses integrating the processors, the L2 cache, the memory controller, the I/O interfaces and bridges, etc. may be integrated onto a single circuit. However, Cho does not disclose or suggest a processor cache unit and a chipset cache controller internal to the processor and the chipset cache being internal to the memory controller which is external to the processor. Furthermore, Cho does not disclose the control signals being double or quad-pumped.

Therefore, Applicant believes that independent claims 1, 14, 27 and their respective dependent claims are distinguishable over the cited prior art references.

### B. Claims 3-13, 16-26, 29-32 Are Not Obvious Under Kumar In View of Cho, Further In View of Lentz and Further In View of Gilda.

In the final Office Action dated February 11, 2004, the Examiner rejected claims 3-13, 16-26, and 29-32 under 35 U.S.C. §103(a) as being unpatentable over Kumar in view of Cho and further in view of Lentz and further in view of U.S. Patent No. 6,438,657 issued to Gilda ("Gilda"). Applicant respectfully traverses the rejection and contends that the Examiner has not met the burden of establishing a prima facie case of obviousness.

Kumar discloses a cache memory with reduced latency by paralleling various memory accesses initiated by the execution unit as discussed above. Cho discloses an out of order associative queue in two clock domains as discussed above. Lentz discloses a system and method for supporting a multiple width memory subsystem as discussed above.

Gilda discloses a pipelined snooping of multiple L1 cache lines. An L2 cache control unit provides the processor with access to a private L2 cache (Gilda, col. 11, lines 55-61).

Kumar, Cho, Lentz and Gilda, taken alone or in any combination, does not disclose, suggest, or render obvious controlling cache memory in an external chipset via double-pumped or quad-pumped control signals and maintaining cache coherency according to an MESI coherence protocol.

There is no motivation to combine Kumar, Cho, Lentz and Gilda because none of them addresses the problem of controlling cache memory in an external chipset and maintain cache coherency. There is no teaching or suggestion that double-pumped or quad-pumped control signals are present. Kumar, read as a whole, does not suggest the desirability of controlling cache memory in an external chipset via double-pumped or quad-pumped control signals and maintaining cache coherency.

Kumar, Cho, and Lentz are discussed above. Gilda merely discloses an L2 cache control unit to provide a processor with access to a private L2 cache plus access to memory through a system bus (Gilda, col. 11, lines 55-59). Gilda does not disclose or suggest the L2 cache being internal to a memory controller. Gilda does not disclose or suggest a chipset cache controller to control a chipset cache located in a chipset via control signals and the chipset cache controller having a coherence controller to maintain coherency according to a MESI coherence protocol. Gilda merely discloses a complex buffer structure to handle the commands from the data/instructions cache units, address translation unit, and system bus via processor interface unit (Gilda, col. 11, lines 62-65). Although the MESI protocol is well known, Gilda does not disclose or suggest the use of control signals from the processor to control a chipset cache internal to a memory controller as recited in claims 1, 14, and 27.

In the present invention, the cited references do not expressly or implicitly suggest controlling cache memory in an external chipset via double-pumped or quad-pumped control signals and maintaining cache coherency according to a coherence protocol. In

addition, the Examiner failed to present a convincing line of reasoning as to why a combination of Kumar, Cho, Lentz and Gilda is an obvious application of controlling cache memory in external chipset.

Therefore, Applicant believes that claims 3-13, 16-26, and 29-32 are distinguishable over the cited prior art references.

## IX. CONCLUSION

The Examiner failed to establish a prima facie case of obviousness and failed to show there is teaching, suggestion or motivation to combine the references in rejecting claims 1-32. "When determining the patentability of a claimed invention which combined two known elements, 'the question is whether there is something in the prior art as a whole suggest the desirability, and thus the obviousness, of making the combination.'" In re Beattie, Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 730 F.2d 1452, 1462, 221 USPQ (BNA) 481, 488 (Fed. Cir. 1984). To defeat patentability based on obviousness, the suggestion to make the new product having the claimed characteristics must come from the prior art, not from the hindsight knowledge of the invention. Interconnect Planning Corp. v. Feil, 744 F.2d 1132, 1143, 227 USPQ (BNA) 543, 551 (Fed. Cir. 1985). To prevent the use of hindsight based on the invention to defeat patentability of the invention, this court requires the Examiner to show a motivation to combine the references that create the case of obviousness. In other words, the Examiner must show reasons that a skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the prior elements from the cited prior references for combination in the manner claimed. In re ROUFFET, 149 F.3d 1350 (Fed. Cir. 1996), 47 USPQ 2d (BNA) 1453. "To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or implicitly suggest the claimed invention or the Examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references." Ex parte Clapp, 227 USPQ 972, 973. (Bd.Pat.App.&Inter. 1985).

In the present invention, Kumar, Cho, Lentz and Gilda, taken alone or in any combination, do not disclose, expressly or implicitly, suggest, or render obvious (1) a chipset cache controller internal to a processor to control a chipset cache via control

signals, (2) the chip set cache being internal to a memory controller, (3) the memory controller being external to the processor, (4) the control signals being double-pumped or quad-pumped, (5) the chipset cache controller having a coherence controller to maintain cache coherency according to a coherence protocol such as the MESI protocol. In addition, the Examiner failed to present a convincing line of reasoning as to why a combination of Kumar, Cho, Lentz and Gilda is an obvious application of controlling cache memory in external chipset using processor.

As a result, none of the cited references discloses, explicitly or implicitly, suggests, or renders obvious the present invention as recited in claims 1-32.

Applicant respectfully request that the Board enter a decision overturning the Examiner's rejection of all pending claims, and holding that the claims are neither anticipated or rendered obvious by the prior art.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: July 1, 2004

THINH V. NGUYEN
Reg. No. 42,034

12400 Wilshire Blvd., 7th Floor
Los Angeles, CA 90025-1026
(714) 557-3800

## X. APPENDIX

The claims of the present application which are involved in this appeal are as follows:

1. (previously presented) An apparatus comprising:

a processor cache unit to process a cache access request from a processor core of a processor, the processor cache unit including a processor cache controller and a processor cache; and

a chipset cache controller internal and coupled to the processor cache unit internally to the processor to control a chipset cache located in a chipset via control signals that are double-pumped or quad-pumped in response to the cache access request from the processor core, the chipset being a memory controller external and coupled to the processor via a bus.

2. (original) The apparatus of claim 1 wherein the chipset cache controller comprises:

a chipset cache tag store to store tags corresponding to cache lines of the chipset cache; and

a coherency controller coupled to the chipset cache tag store to maintain cache coherency among the processor cache, the chipset cache, and a memory, according to a coherence protocol.

3. (original) The apparatus of claim 2 wherein the coherency protocol is a modified, exclusive, share, and invalidated (MESI) protocol.

4. (previously presented) The apparatus of claim 3 wherein the coherence controller comprises:

a chipset interface circuit to send the control signals to the chipset according to cache state and type of the cache access request, the control signals specifying an operation performed by the chipset.

5. (original) The apparatus of claim 4 wherein the control signals include at least a set identifier for a cache set in the chipset cache corresponding to the cache access request, a cache valid indicator asserted when a cache line in the cache set is valid, and a flush indicator asserted when the cache line is flushed.

6. (original) The apparatus of claim 5 wherein when the type of the cache access request is a read request and the cache valid indicator is not asserted, the operation includes one of a transfer of a data read from the memory to the cache set in the chipset cache and a transfer of a data read from the memory to the processor.

7. (original) The apparatus of claim 6 wherein when the flush indicator is asserted, the operation further includes a flushing of existing data at the cache set.

8. (original) The apparatus of claim 4 wherein when the type of the cache access request is a read request and the cache valid indicator is asserted, the operation includes a transfer of a data read from the cache set to the processor.

9. (original) The apparatus of claim 4 wherein when the type of the cache access request is a write request, the operation includes a transfer of a data from the processor to the cache set in the chipset cache.

10. (original) The apparatus of claim 9 wherein when the cache valid indicator is not asserted, the operation further includes a transfer of the data from the processor to the memory.

11. (original) The apparatus of claim 9 wherein when the flush indicator is asserted, the operation further includes a flushing of existing data at the cache set.

12. (original) The apparatus of claim 5 further comprising:

a snoop circuit coupled to the chipset cache tag store to check if an address snooped on the bus matches with one of entries in the chipset cache tag store.

13. (original) The apparatus of claim 12 wherein the set identifier specifies the cache set corresponding to the one of the entries that matches the address snooped on the bus.

14. (previously presented) A method comprising:

processing a cache access request from a processor core of a processor by a processor cache unit, the processor cache unit including a processor cache controller and a processor cache; and

controlling a chipset cache located in a chipset by a chipset cache controller internal to the processor via control signals that are double-pumped or quad-pumped in response to the cache access request from the processor core, the chipset being a memory controller external and coupled to the processor via a bus.

15. (original) The method of claim 14 wherein controlling the chipset cache comprises:

storing tags corresponding to cache lines of the chipset cache in a chipset cache tag store; and

maintaining cache coherency among the processor cache, the chipset cache, and a memory, according to a coherence protocol.

16. (original) The method of claim 15 wherein the coherency protocol is a modified, exclusive, share, and invalidated (MESI) protocol.

17. (previously presented) The method of claim 16 wherein maintaining cache coherency comprises:

sending the control signals to the chipset according to cache state and type of the cache access request, the control signals specifying an operation performed by the chipset.

18. (original) The method of claim 17 wherein the control signals include at least a set identifier for a cache set in the chipset cache corresponding to the cache access request, a cache valid indicator asserted when a cache line in the cache set is valid, and a flush indicator asserted when the cache line is flushed.

19. (original) The method of claim 18 wherein when the type of the cache access request is a read request and the cache valid indicator is not asserted, the operation includes one of a transfer of a data read from the memory to the cache set in the chipset cache and a transfer of a data read from the memory to the processor.

20. (original) The method of claim 19 wherein when the flush indicator is asserted, the operation further includes a flushing of existing data at the cache set.

21. (original) The method of claim 17 wherein when the type of the cache access request is a read request and the cache valid indicator is asserted, the operation includes a transfer of a data read from the cache set to the processor.

22. (original) The method of claim 17 wherein when the type of the cache access request is a write request, the operation includes a transfer of a data from the processor to the cache set in the chipset cache.

23. (original) The method of claim 22 wherein when the cache valid indicator is not asserted, the operation further includes a transfer of the data from the processor to the memory.

24. (original) The method of claim 22 wherein when the flush indicator is asserted, the operation further includes a flushing of existing data at the cache set.

25. (original) The method of claim 18 further comprising:

checking if an address snooped on the bus matches with one of entries in the chipset cache tag store.

26. (original) The method of claim 25 wherein the set identifier specifies the cache set corresponding to the one of the entries that matches the address snooped on the bus.

27. (previously presented) A system comprising:

a memory to store data;

a chipset coupled to memory having a chipset cache, the chipset being a memory controller; and

a processor coupled to the memory and the chipset via a bus, the processor including a processor core and a cache unit, the cache unit comprising:

a processor cache unit to process a cache access request from the processor core, the processor cache unit including a processor cache controller and a processor cache, and

a chipset cache controller coupled to the processor cache unit to control the chipset cache via control signals that are double-pumped or quad-pumped in response to the cache access request from the processor core.

28. (original) The system of claim 27 wherein the chipset cache controller comprises:

a chipset cache tag store to store tags corresponding to cache lines of the chipset cache; and

a coherency controller coupled to the chipset cache tag store to maintain cache coherency among the processor cache, the chipset cache, and a memory, according to a coherence protocol.

29. (original) The system of claim 28 wherein the coherency protocol is a modified, exclusive, share, and invalidated (MESI) protocol.

30. (previously presented) The system of claim 29 wherein the coherence controller comprises:

a chipset interface circuit to send the control signals to the chipset according to cache state and type of the cache access request, the control signals specifying an operation performed by the chipset.

31. (original) The system of claim 30 wherein the control signals include at least a set identifier for a cache set in the chipset cache corresponding to the cache access request, a cache valid indicator asserted when a cache line in the cache set is valid, and a flush indicator asserted when the cache line is flushed.

32. (original) The system of claim 31 wherein the cache unit further comprising:

a snoop circuit coupled to the chipset cache tag store to check if an address snooped on the bus matches with one of entries in the chipset cache tag store.